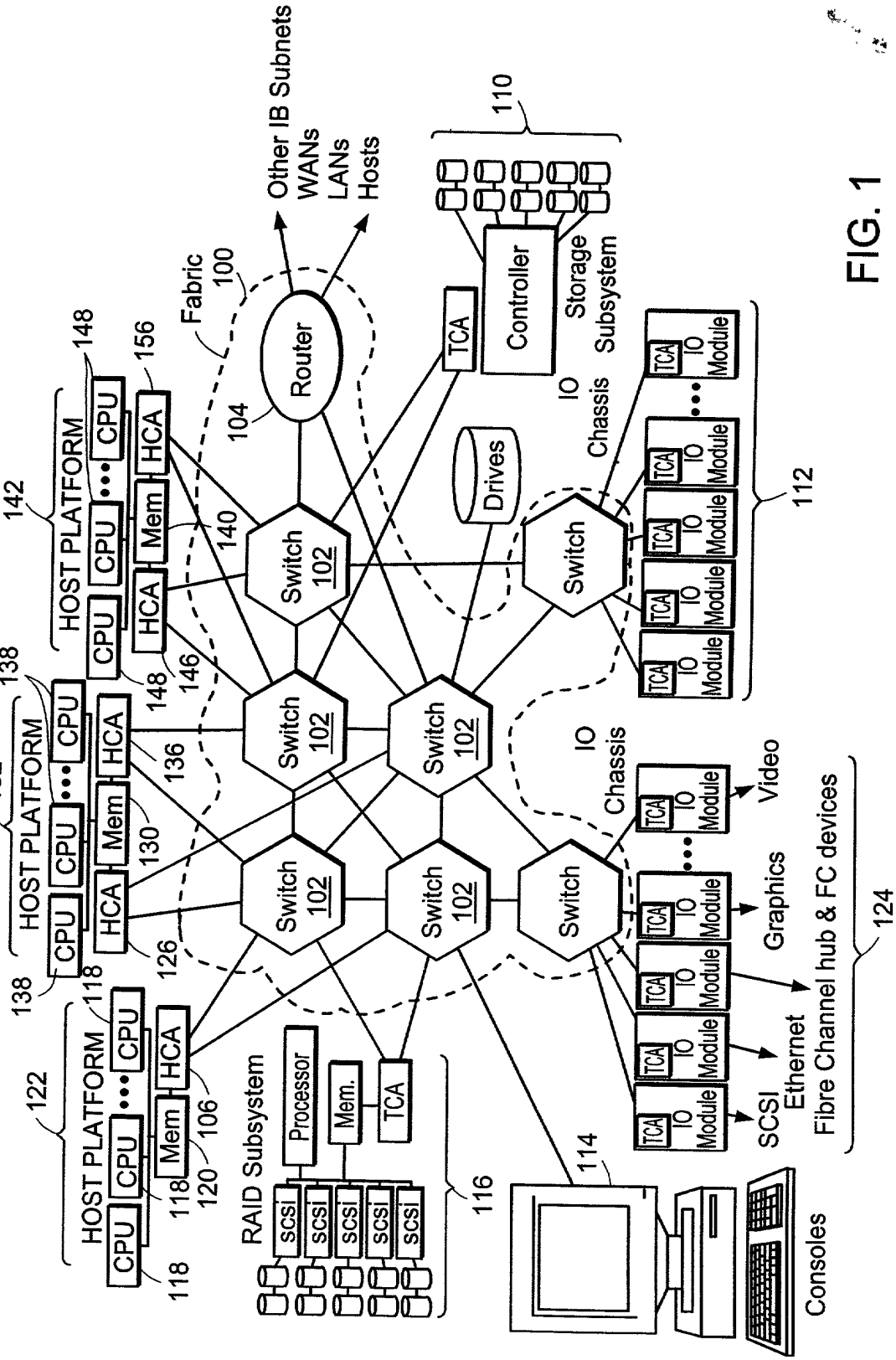
Other IB Subnets
WANs
LANs
Hosts
Fabric
100
Router
104
110
Controller
Storage Subsystem
TCA
IO Chassis
Drives
Switch
102
112
IO Module
HOST PLATFORM
CPU
HCA
Mem
132
138
142
148
156
140
146
136
130
126
118
122
106
120
RAID Subsystem
Processor
Mem.
scsi
116
114
Consoles
Video
Graphics
SCSI
Ethernet
Fibre Channel hub & FC devices
124

FIG. 1

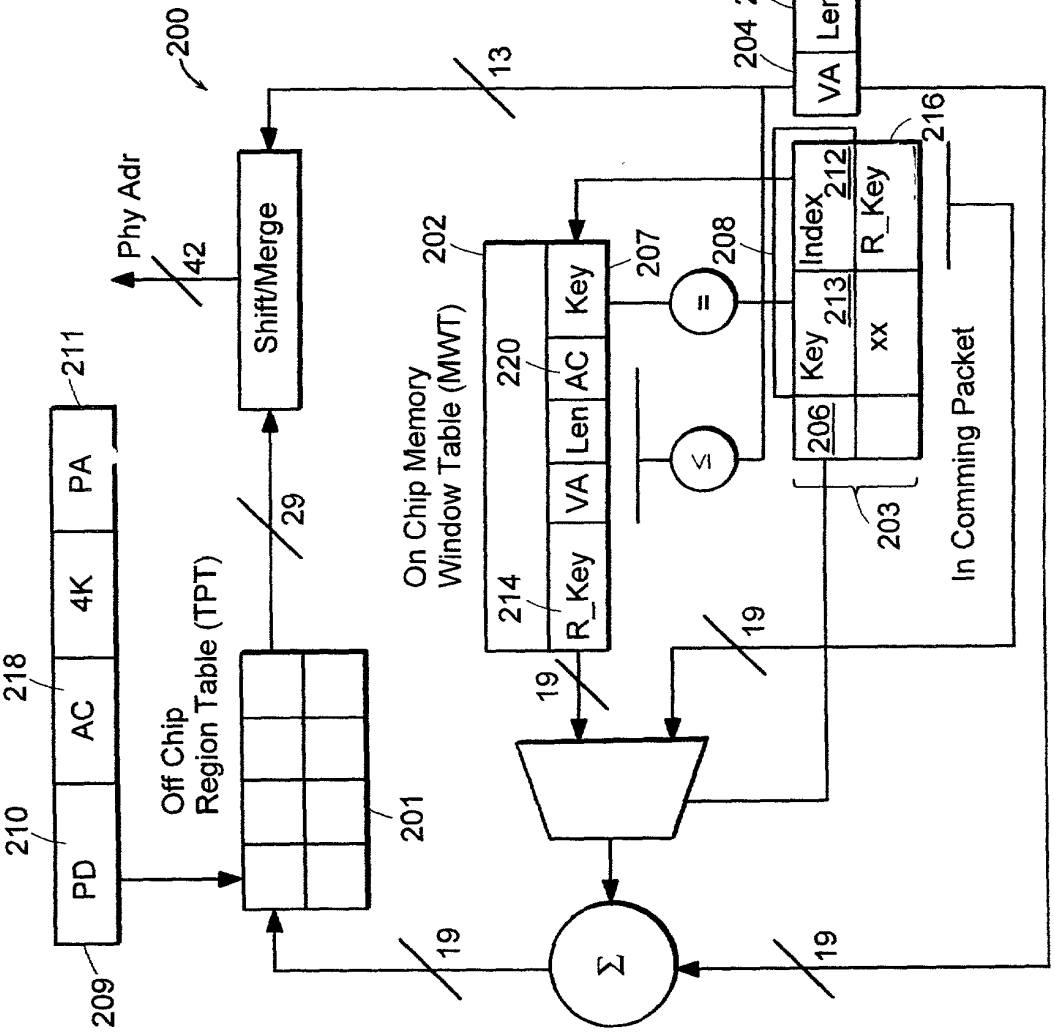
200
Phy Adr
42
Shift/Merge
13
29
Off Chip
Region Table (TPT)
201
211
PA
4K
AC
PD
218
210
209
On Chip Memory
Window Table (MWT)
202
Key
AC
Len
VA
R_Key
220
214
207
208
=
≤
204 205
Len
VA
216
Index
212
R_Key
Key
213
xx
206
203
In Comming Packet
19
19
19
Σ

FIG. 2

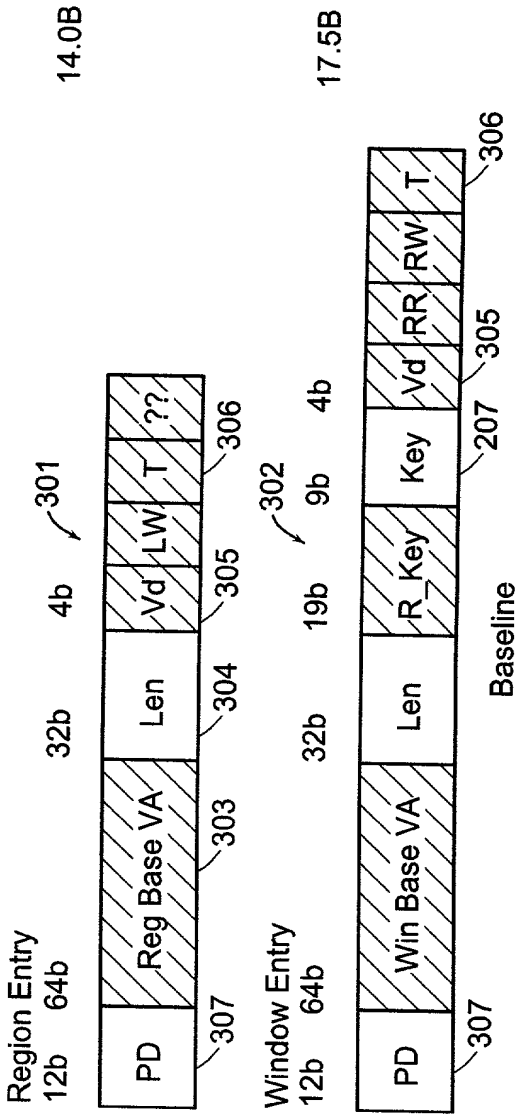
14.0B
17.5B
Region Entry
12b 64b
32b 4b
301
PD
Reg Base VA
Len
Vd
LW
T
??
303
304
305
306
307
Window Entry
12b 64b
32b 19b 9b 4b
302
PD
Win Base VA
Len
R_Key
Key
Vd
RR
RW
T
207
305
306
307
Baseline

FIG. 3

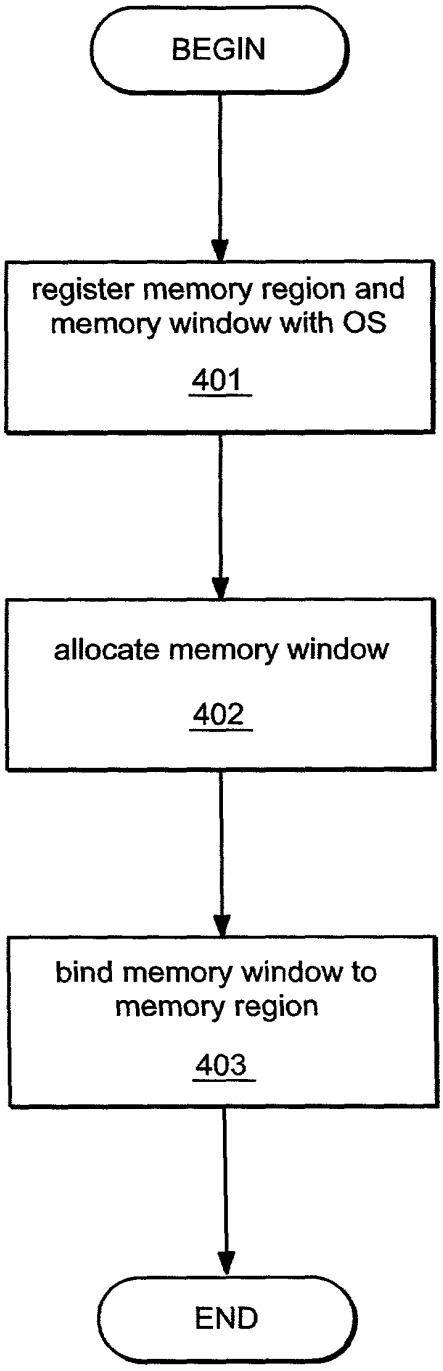

FIG.4

EXPRESS MAIL NO. EV 339 954 245 US

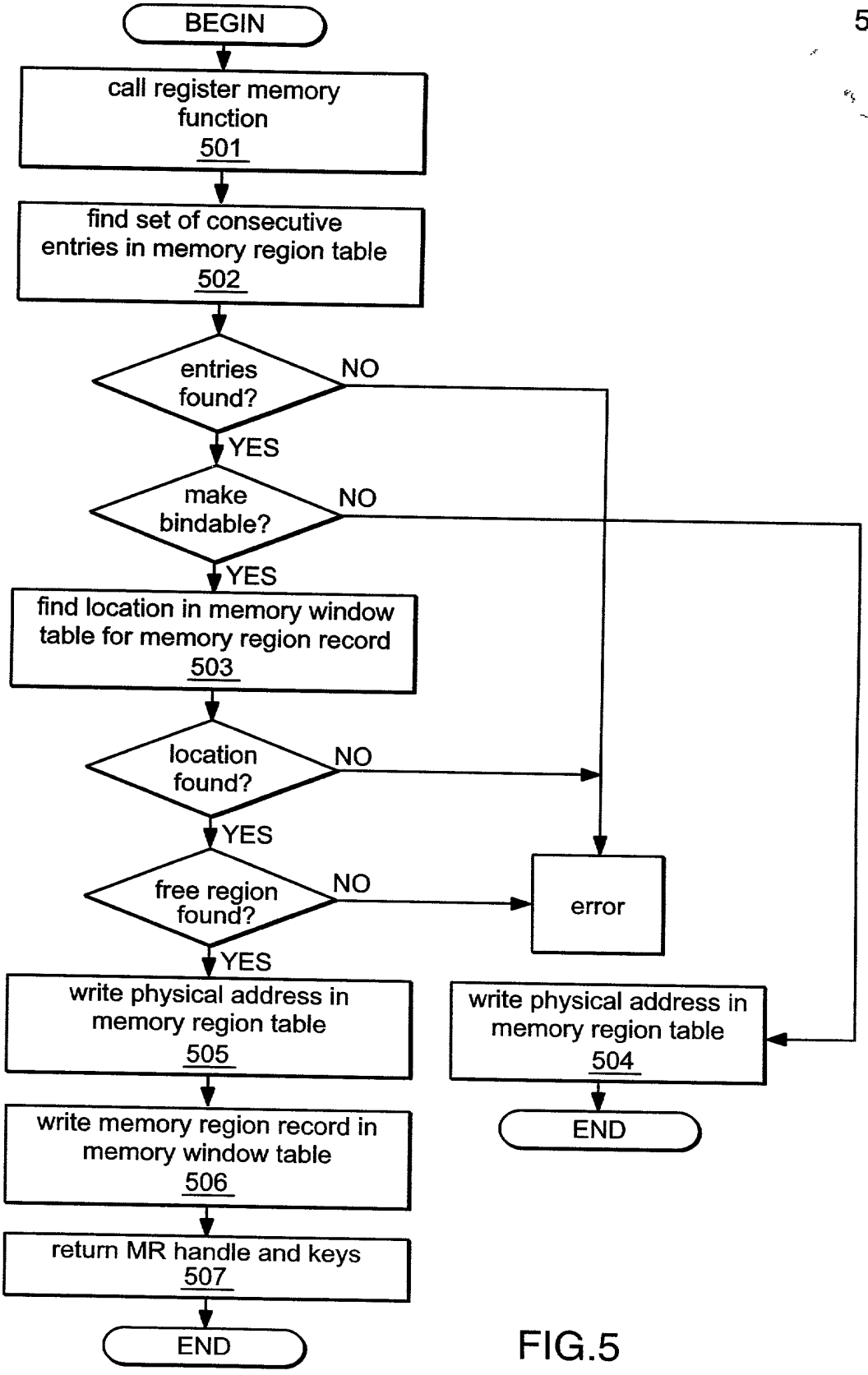
BEGIN
call register memory function 501
find set of consecutive entries in memory region table 502
entries found?
NO
YES
make bindable?
NO
YES
find location in memory window table for memory region record 503
location found?
NO
YES
free region found?
NO
YES
error
write physical address in memory region table 505
write memory region record in memory window table 506
return MR handle and keys 507
END
write physical address in memory region table 504
END

FIG.5

Jul 15, 2004 2:50 PM

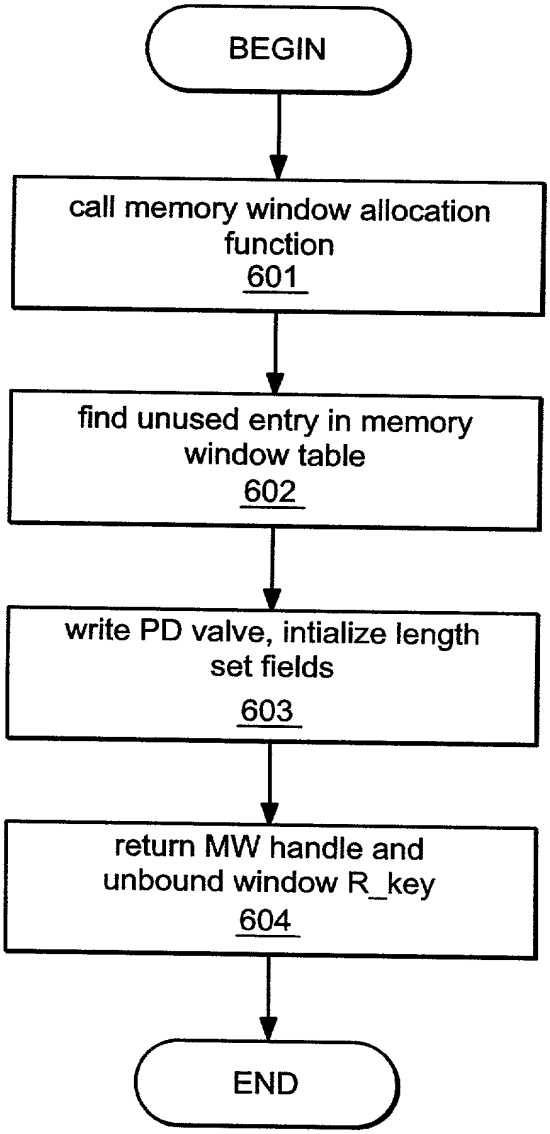

FIG.6

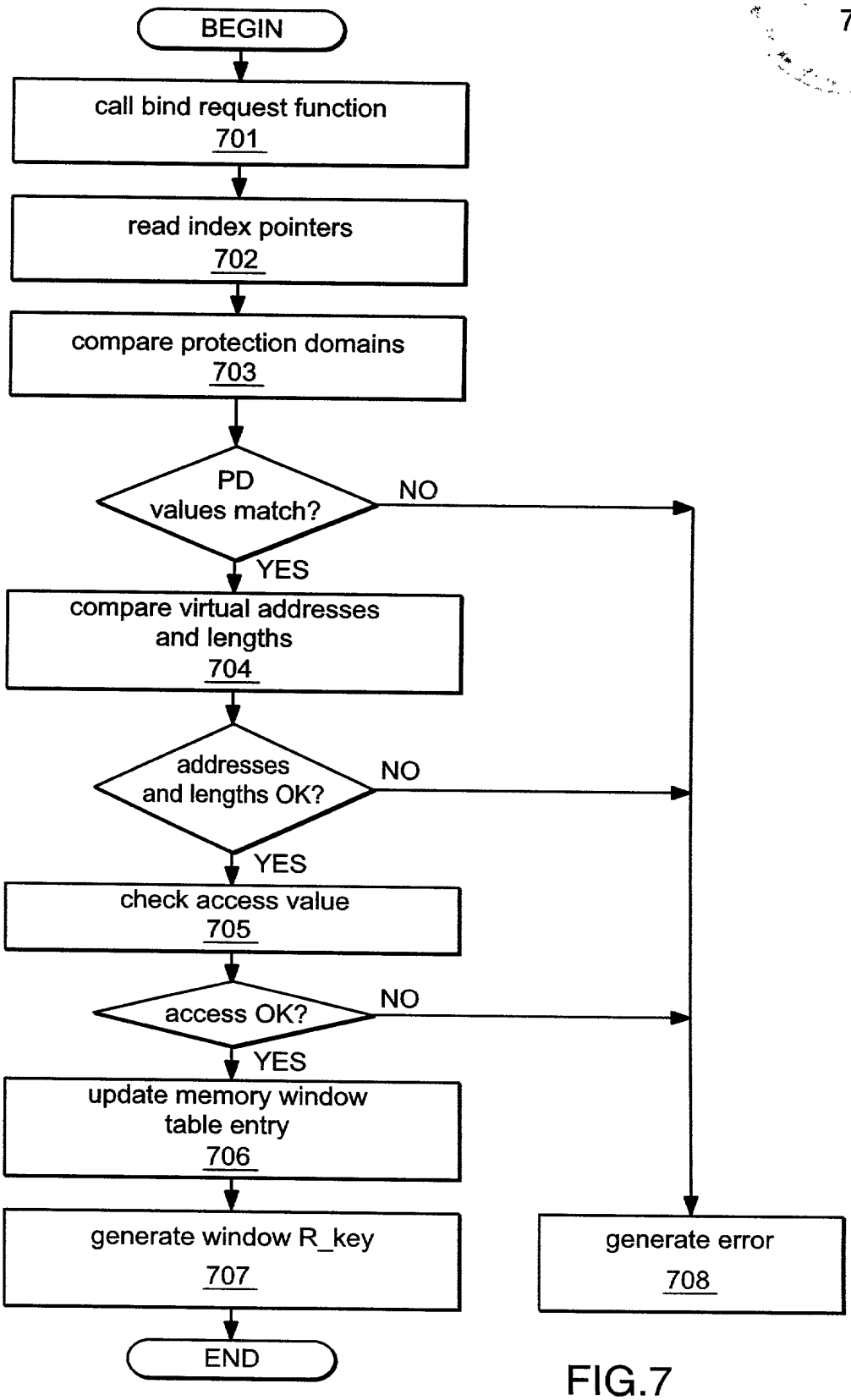
BEGIN
call bind request function
701
read index pointers
702
compare protection domains
703
PD
values match?
NO
YES
compare virtual addresses
and lengths
704
addresses
and lengths OK?
NO
YES
check access value
705
access OK?
NO
YES
update memory window
table entry
706
generate window R_key
707
END
generate error
708

FIG.7

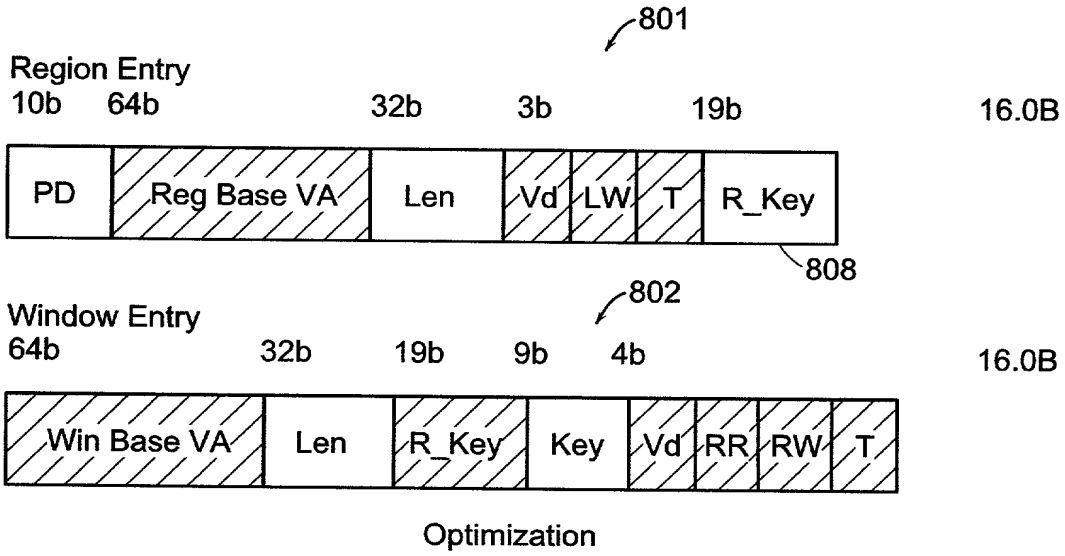
801
Region Entry
10b
64b
32b
3b
19b
16.0B
PD
Reg Base VA
Len
Vd
LW
T
R_Key
808
802
Window Entry
64b
32b
19b
9b
4b
16.0B
Win Base VA
Len
R_Key
Key
Vd
RR
RW
T
Optimization

FIG. 8

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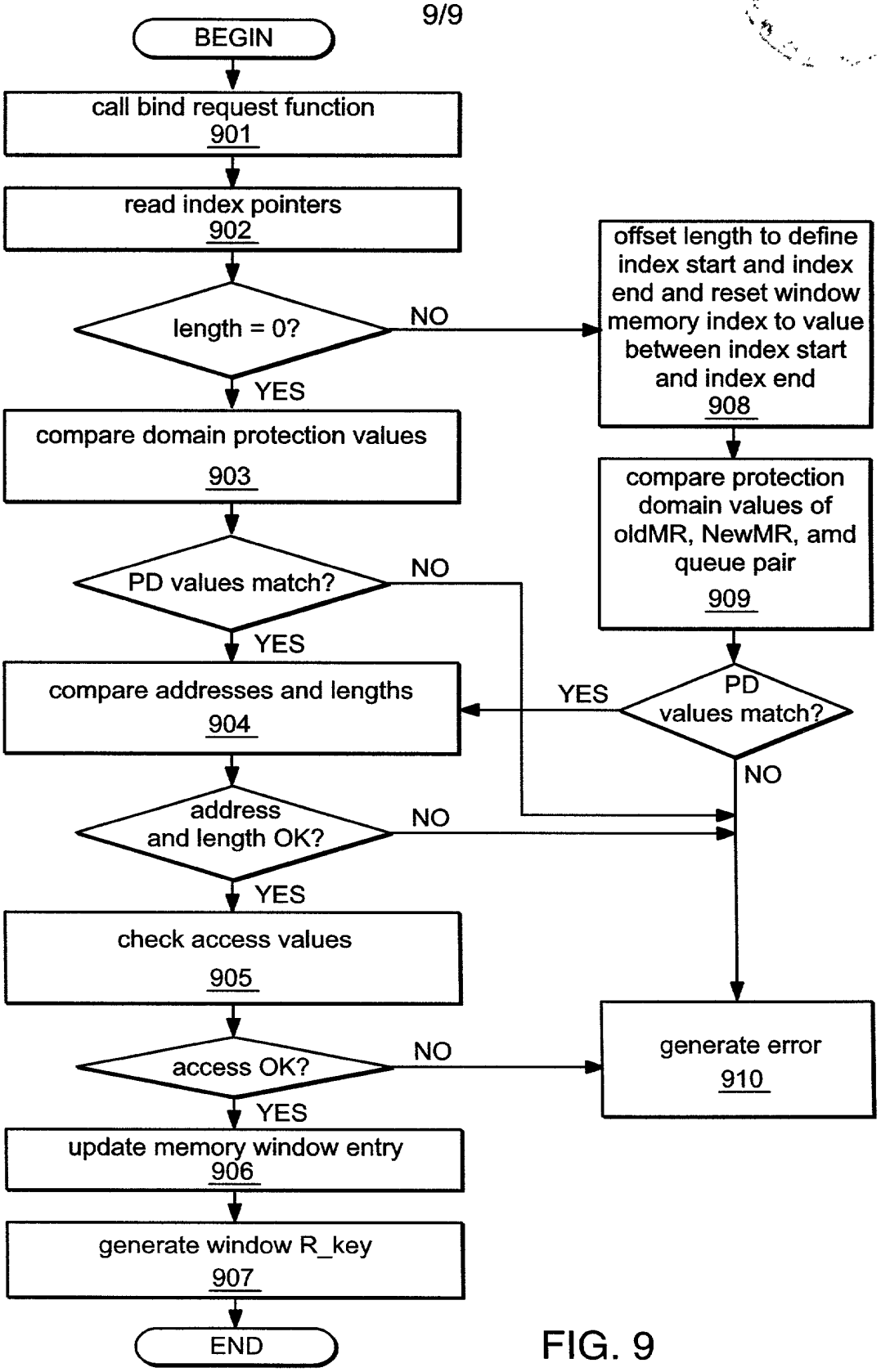
BEGIN
call bind request function
901
read index pointers
902
length = 0?
NO
YES
offset length to define index start and index end and reset window memory index to value between index start and index end
908
compare domain protection values
903
compare protection domain values of oldMR, NewMR, amd queue pair
909
PD values match?
NO
YES
PD values match?
YES
NO
compare addresses and lengths
904
address and length OK?
NO
YES
check access values
905
access OK?
NO
YES
generate error
910
update memory window entry
906
generate window R_key
907
END

FIG. 9